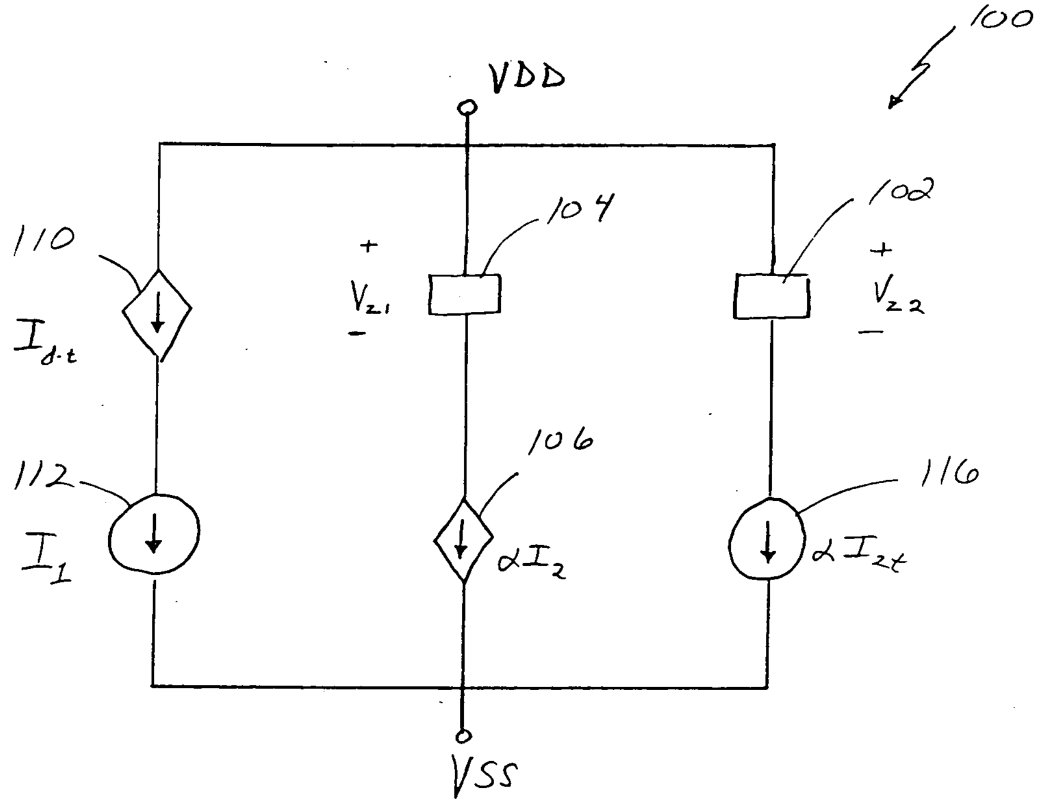

FIG. 1

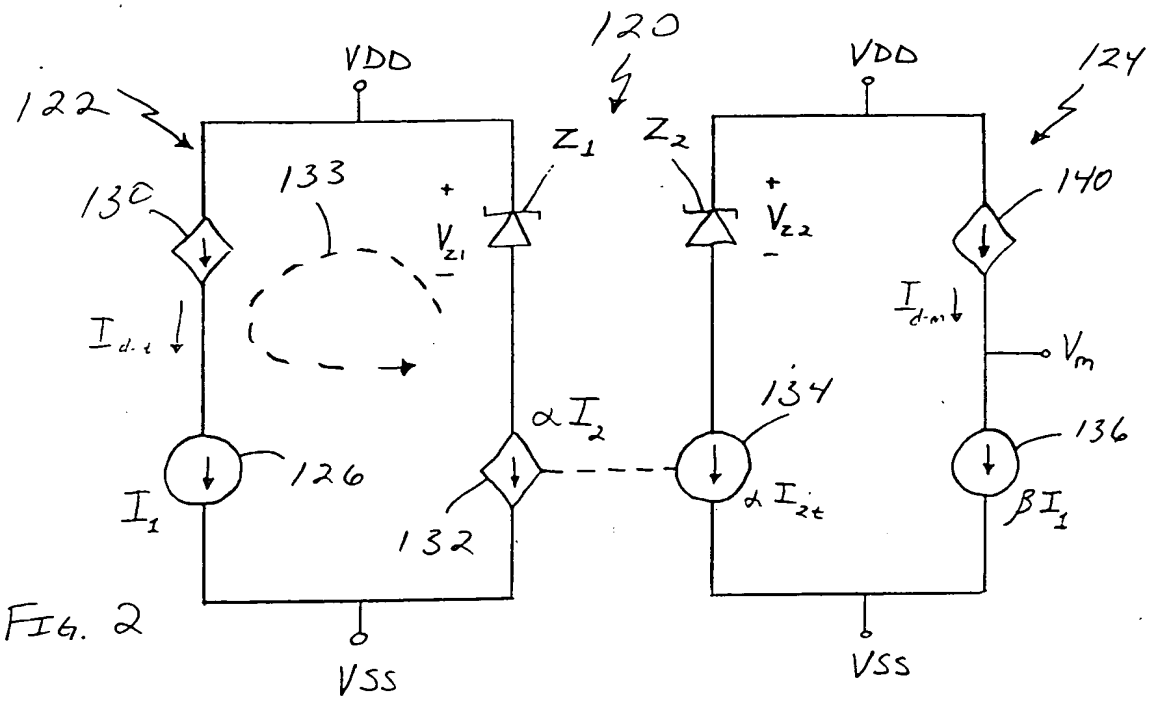
120
VDD
122
VDD
124
Z1
Z2
133
130
140
V_{z1}
V_{z2}
I_{d-t}
I_{d-m}
V_m
134
αI_2
136
126
I_1
αI_{2t}
βI_1
132
VSS
VSS

FIG. 2

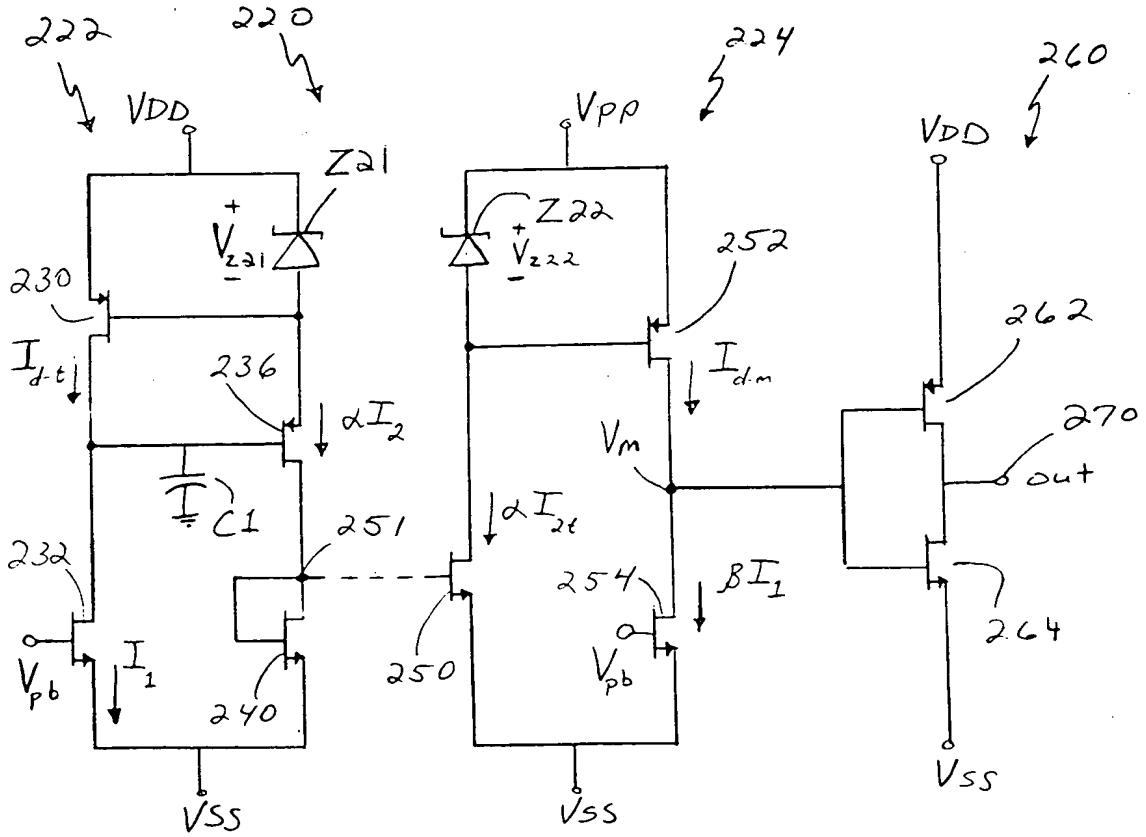
222
220
224
260
VDD
Vpp
VDD
Z21
Z22
V_{z21}
V_{z22}
230
252
262
I_{d-t}
236
αI_2
I_{d-m}
270
V_m
out
C1
αI_{2t}
251
232
254
βI_1
V_{pb}
I_1
240
250
V_{pb}
264
VSS
VSS
VSS

FIG. 3

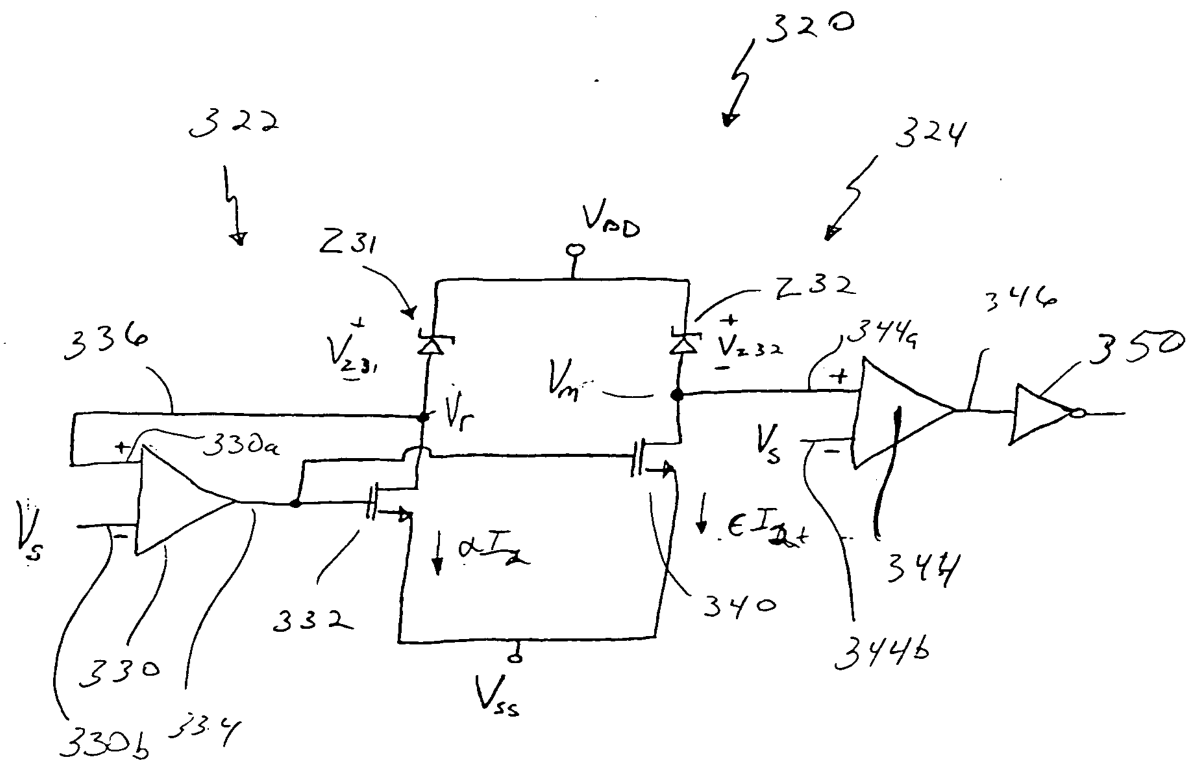

FIG. 4

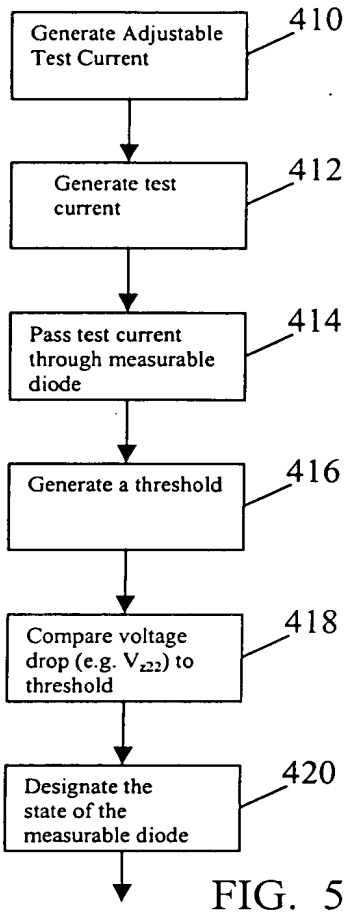

FIG. 5

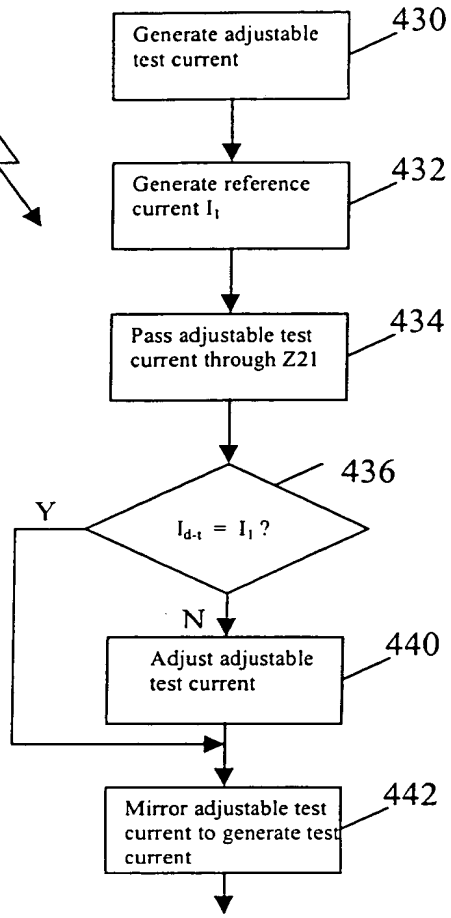

FIG. 6

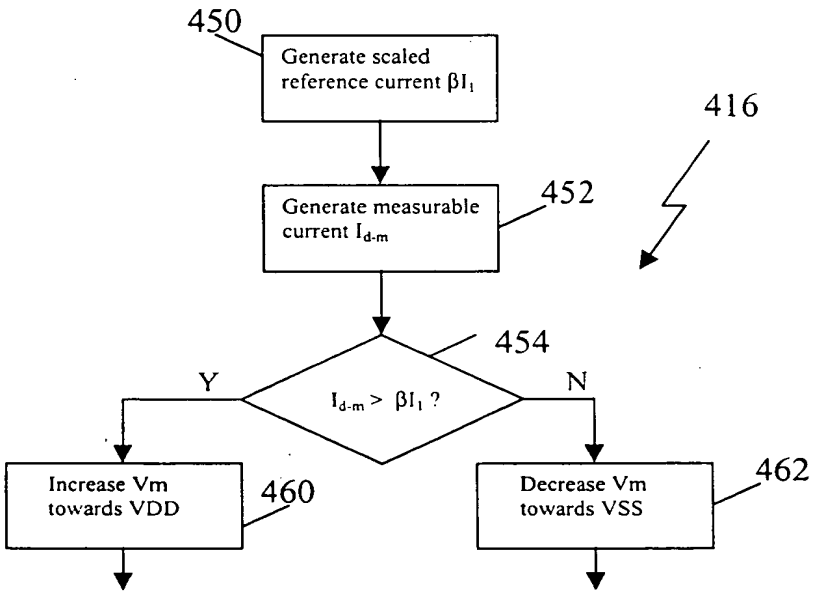

FIG. 7

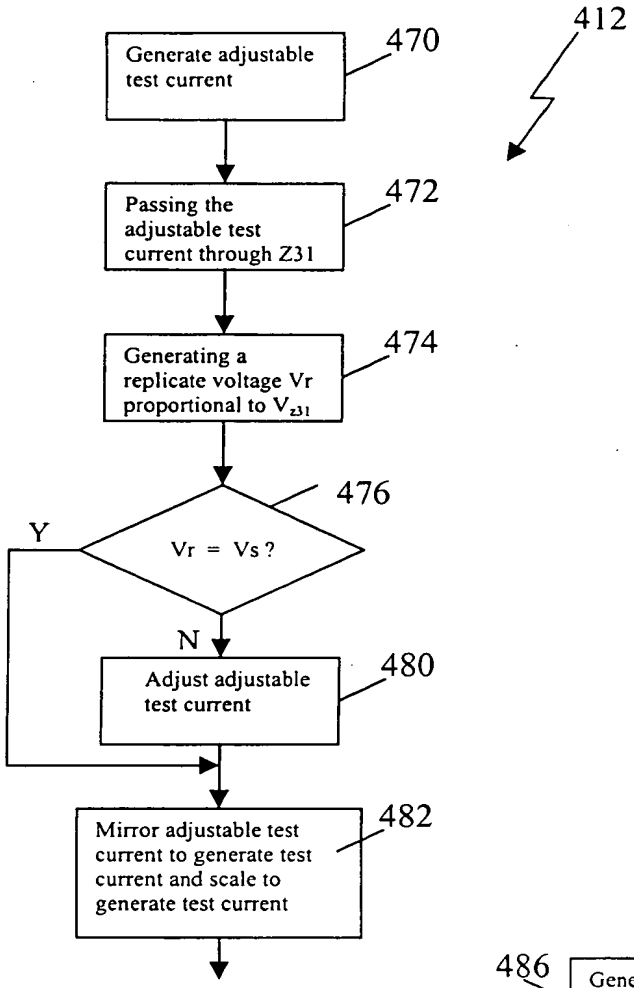
412
Generate adjustable test current
470
Passing the adjustable test current through Z31
472
Generating a replicate voltage Vr proportional to V_{z31}
474
476
Vr = Vs ?
Y
N
Adjust adjustable test current
480
Mirror adjustable test current to generate test current and scale to generate test current
482

FIG. 8

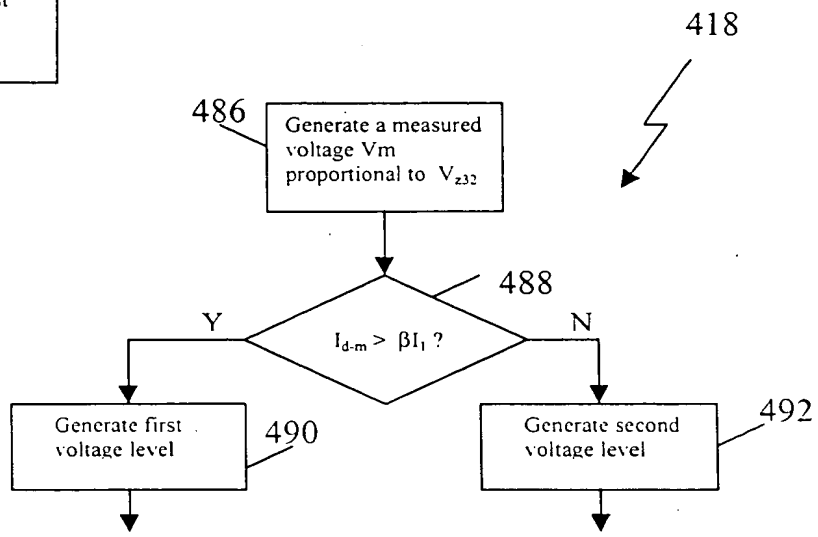
418
486
Generate a measured voltage Vm proportional to V_{z32}
488
$I_{d-m} > \beta I_1$?
Y
N
Generate first voltage level
490
Generate second voltage level
492

FIG. 9

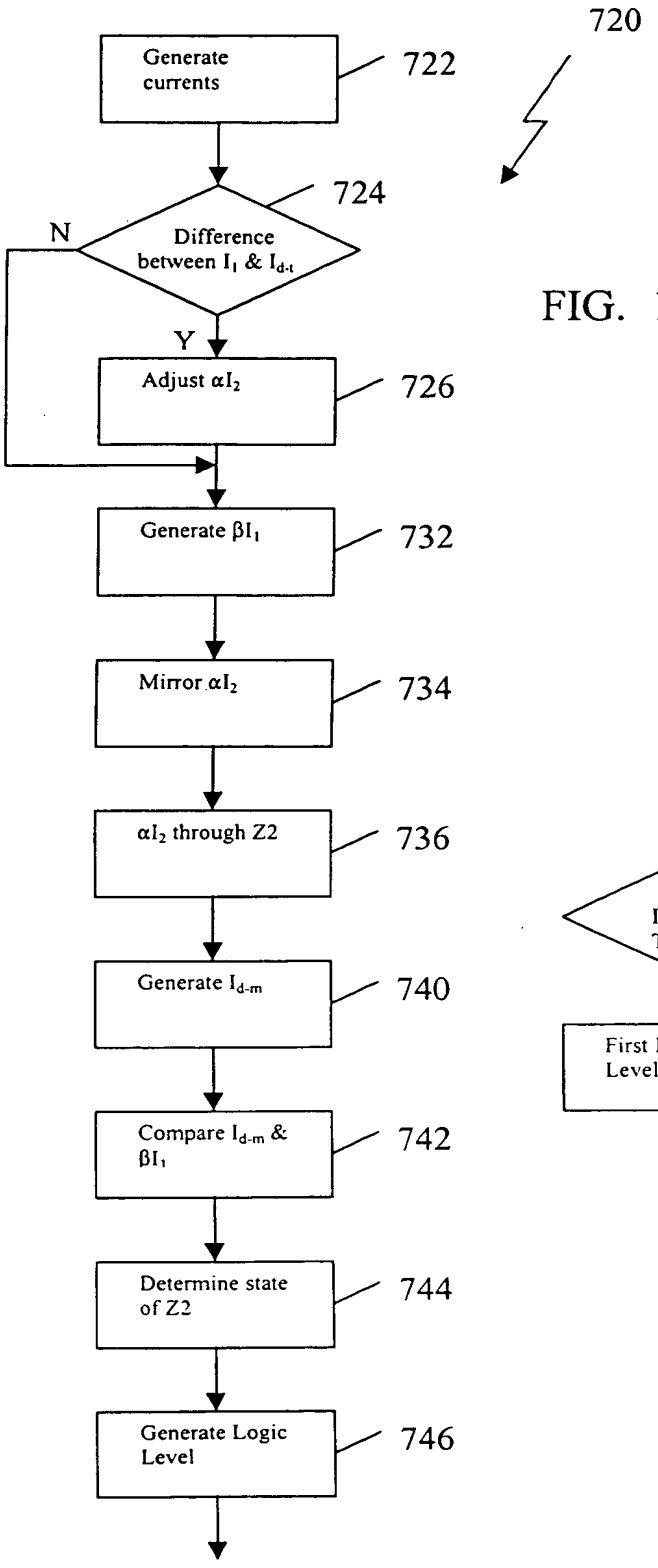
720
Generate currents
722
724
Difference between I_1 & I_{d-t}
N
Y
Adjust αI_2
726
Generate βI_1
732
Mirror αI_2
734
αI_2 through Z2
736
Generate I_{d-m}
740
Compare I_{d-m} & βI_1
742
Determine state of Z2
744
Generate Logic Level
746

FIG. 10

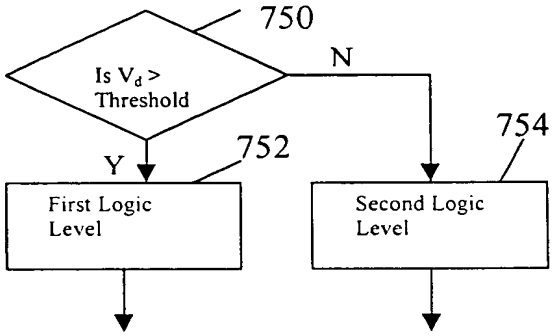
750
Is V_d > Threshold
N
Y
752
754
First Logic Level
Second Logic Level

FIG. 11